MPC5500 Family of New Generation Embedded Controllers

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This article describes the recently announced new generation of PowerPC™ embedded controllers, the MPC5500 Family. The MPC5500 family will be powered by the 'e500' CPU and will be integrated with high performance peripherals and Flash EEPROM memory. One of the key characteristics of the e500 CPU is the ability to implement 'Application Processing Units' (APUs) – the concept of such units and their basic functionality will also be described in this article.

The MPC5500 name hints that the new embedded controller family is an evolution of today's popular MPC500 Family. This means that the software that has been written for the MPC500 devices will be upwards code compatible with the MPC5500 devices. In order to explain the significance of the technological advances of the new embedded controller family, it is first necessary to indulge in a brief history lesson. Figure 1 illustrates the evolution of embedded controllers from Motorola that have been regarded as 'industry standards'.

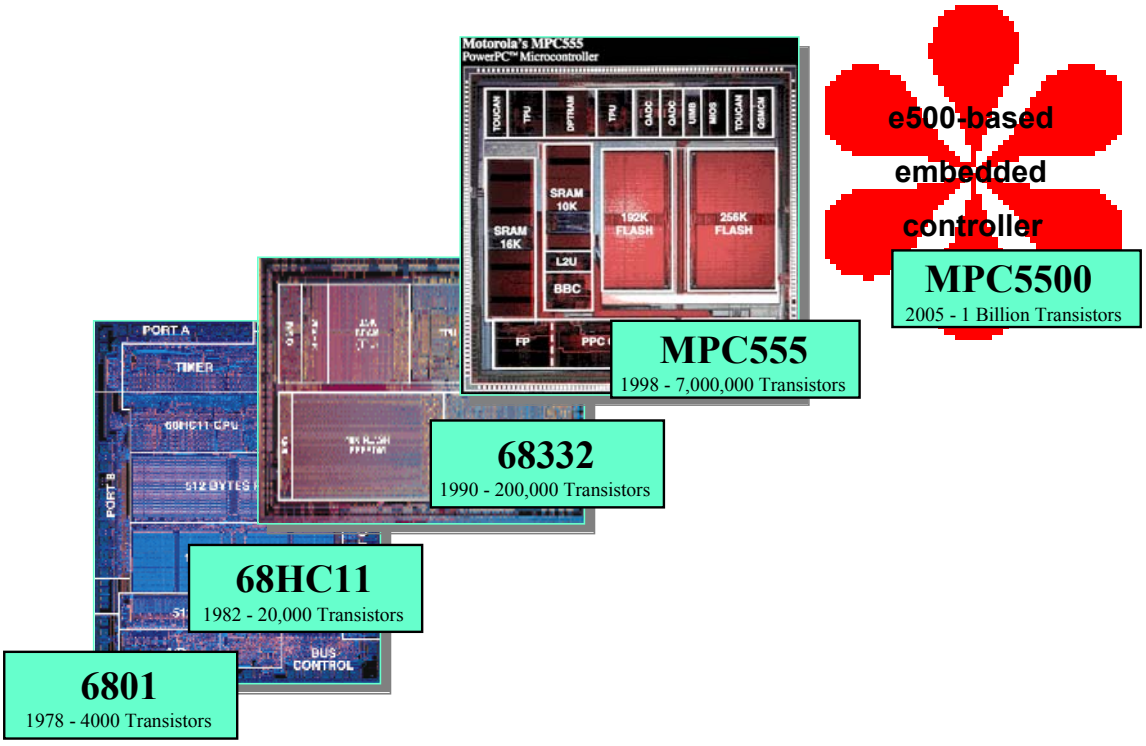


Figure 1 – Industry Standard Embedded Controller Evolution

The Figure illustrates the development of five generations of embedded controller families, all of which can still be found in products used today. The 6801 was introduced in 1978 and the latest, the MPC5500 (based on the 'e500' Central Processing Unit) was announced in 2001. In this

period of time, the transistor count for these devices has grown from around 4000 to over one billion by the middle of this decade.

All of the families of embedded controllers shown in the diagram have been used in automotive engine control systems. Although these families of embedded controllers are used in many other types of systems, the position of 'industry standard' in automotive engine control is significant. This is one of the most control intensive systems anywhere and there is a strong requirement to provide very high performance for a relatively low cost.

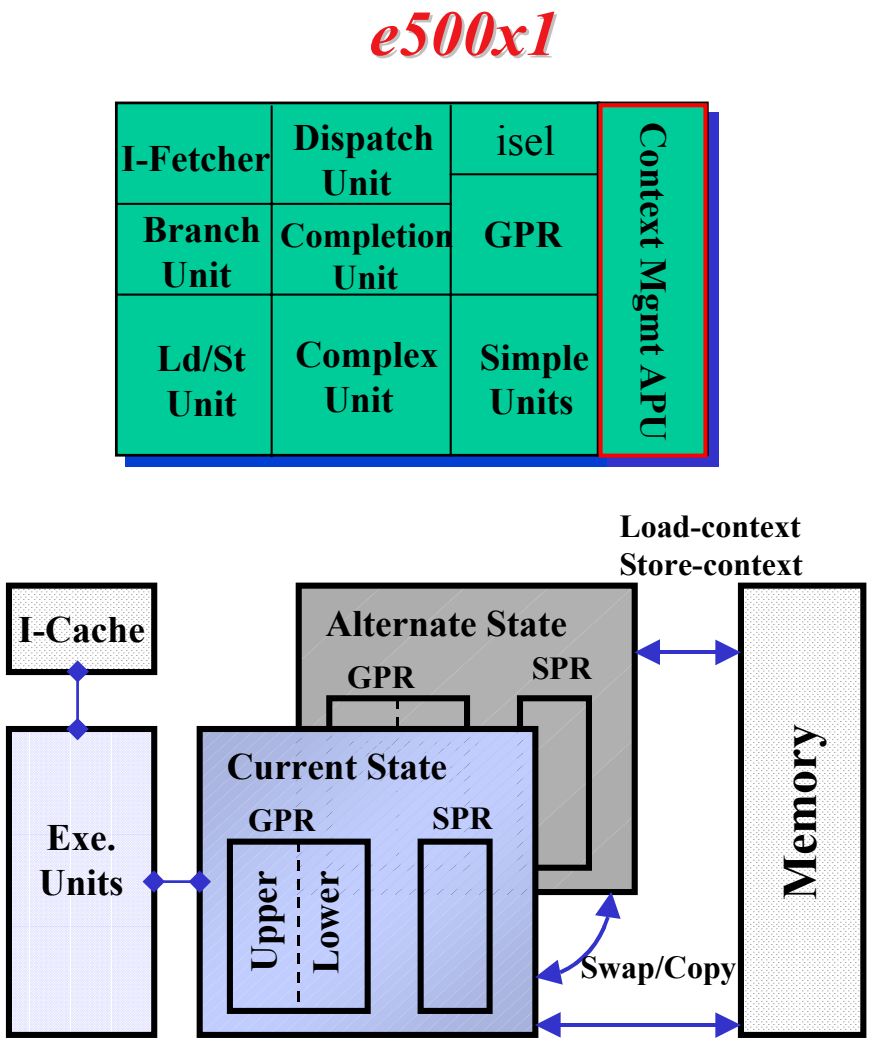


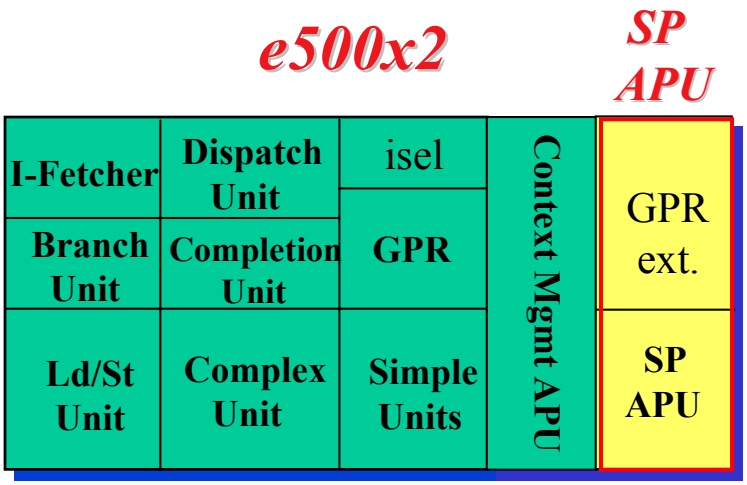
Figure 2 – e500 CPU with Context management APU

Application Processing Units

The growth in complexity of the embedded controllers is down to the growth in memory sizes and integrated peripherals as well as the core, although the development of Central Processor Units since the 6801 has been significant. At the heart of an MPC5500 embedded controller is the e500 CPU. One of the significant developments in this CPU is its ability to implement Application Processing Units (APUs). An APU is a module that can be added to the core to enhance a particular aspect of its performance. Figure 2 illustrates a basic e500 CPU that has a

Context management APU added. This 'flavor' of the e500 CPU has been designated the 'e500x1'.

The top section of Figure 2 illustrates the basic CPU on the left and the Context management block on the right. Below the CPU block diagram is a diagram that describes in more detail the functionality of the APU. The basic CPU includes instruction fetching mechanism, various operation units for execution of basic tasks, General Purpose Registers (GPR) and 'ISEL' block. ISEL stands for '*Integer SELect'* and it is used for branch prediction purposes. In embedded controller code, there is often many branches that the program can take. If a branch is taken, the 'pipeline' that feeds the CPU it is 'flushed'. This results in a performance penalty, as the pipeline has to be refilled with instructions before the code can recommence execution. ISEL hardware is used to remove performance penalties by executing both the 'if' and the 'else' parts of the decision and moving to the desired branch. This is efficient as there are no branch mispredictions.



Performance Examples
(FFT with 32-bit IEEE FP)

1600 MMAC/s peak performance

FFT: radix-4 complex 256 point
with floating-point arithmetic
5076 clock cycles
25 µs at 200 MHz
6.4 µs at 800 MHz

Figure 3 – Signal Processing APU

The concept of the APU will add significant efficiency to the embedded controller family. It means that an APU can be added to the basic CPU in applications that specifically require it. If its not required, then it need not be added or used. This provides a high degree of custom

functionality but retains modularity that allows economies of scale and good common development tool support.

The Context Management APU functionality is shown in the lower half of Figure 2. This APU provides a fast and deterministic response to interrupts. This is important in all sorts of 'real-time' applications where a specific output is required in the event of a pre-determined sensor input signal being detected. At clock speeds of 400Mhz, this interrupt response will be as low as 12 nano seconds. The context switch itself is accomplished by 'swapping out' the General Purpose Registers (GPRs) and Special Purpose Registers (SPRs) that are visible to the CPU.

Figure 3 illustrates another innovation in the CPU by adding another APU for signal processing. This enhancement is identified by designating the 'e500x2' nomenclature. Signal processing in embedded controllers is becoming an option due to the increased clock speeds and reduction in silicon size that allow more circuits for lower costs. Functions like filtering have typically been performed using analog filtering chips or Digital Signal Processors. The Signal Processing APU for the e500 CPU can also handle this function. This results in fewer chips being required – thus leading to lower costs, better performance and greater reliability.

The 'SP APU' shown in Figure 3 illustrates the addition of an extension to the General Purpose Registers as well as the Signal Processing Application Processing Unit. Specifically there are 64 new registers along with 222 new instructions to manipulate data contained within them.

e500 Core Based Implementation

- *e500* core targets different markets with optional APUs implementation
- *e500x1*
  - Network and Communication
  - General purpose controls
  - Real-time application
- *e500x2*
  - Automotive market
  - Real-time application with signal processing capability

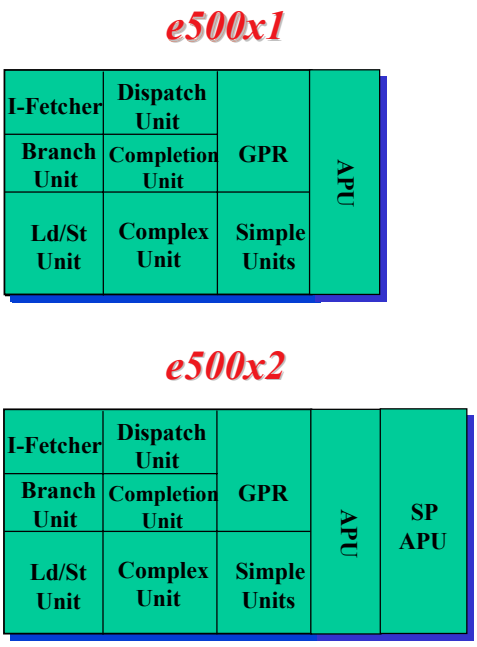


Figure 4 – Application Processing Unit approach

The lower half of Figure 3 illustrates the performance capabilities of the Signal processing APU. Using the integrated IEEE compliant Floating Point (FP) unit, the APU will support up to 1600

million ‘multiply and accumulate’ instructions per second. This is an impressive quotient for an embedded controller. A ‘radix-4’ 256-point Fast Fourier Transform (FFT) algorithm will execute in 5076 clock cycles.

Figure 4 outlines the basic concept by proposing a core that would be best suited to networking and communications (the e500x1) and a core that is optimized for automotive and other control-intensive applications (the e500x2). The automotive core shown in Figure 4 includes the signal processing APU that could be used for an application like filtering the waveforms from engine sensors.

Other Key Design Features

As well as the functionality of the Central Processing Unit, another key defining feature of the MPC5500 family of embedded controllers is the Flash EEPROM memory. There are several reasons why Flash EEPROM is a requirement of a high performance embedded controller that must live up to the popularity of its predecessors. Embedded Flash memory improves performance significantly as there is no big penalties for going ‘off-board’ to a separate memory chip to fetch instructions. This can severely limit performance. Another advantage is that Integrated Flash improves reliability as it reduces chip-count and reduces the number of interconnections in the systems. Typically the number of interconnections is proportional to the number of reliability problems that can be expected. Another thing to consider is that the ability to program Flash memories saves money as high inventory levels of devices with different ROM codes are not required. Inventory costs money.

The MPC5500 Family of embedded controllers is being developed to produce optimal performance for Electromagnetic Compatibility (EMC). There are several on-chip design features that ensure good EMC performance.

EMC is becoming a huge issue for electronic system manufacturers as the operating speed of electronic components is becoming faster (higher frequencies lead to increased electromagnetic emissions). The increasing number of electronic components and sub-systems that could potentially affect each other’s operation is also increasing.

Electromagnetic compatibility can be optimized by careful design of the integrated circuit and the printed circuit board. A system is considered electromagnetically compatible if it has satisfied three criteria:

1) It does not cause interference with other systems
2) It is not susceptible to emissions from other systems
3) It does not generate interference with itself

At the integrated circuit design level, there are many considerations which can enhance the EMC performance of the design: Using less clocks and turning off clocks when not in use, reducing output power buffer drive, using multiple power and ground pins and reducing internal trace impedance on these pins, eliminating integrated charge pump circuitry and positioning high frequency signals next to a ground bus are all steps which are now taken to improve EMC.

In addition the MPC5500 Family uses a phase-locked loop input clock circuit that ramps down the clock frequency to reduce emissions when full-speed operation is not required.

Conclusion

A new family of embedded controllers must be developed with a delicate balancing act in mind. On one hand, the device must retain as much compatibility as possible. This is required to re-use existing software from the previous generation of embedded controller. There is on the other hand, little point in merely rolling out the same old embedded controller family with a new name– for this reason, significant enhancements are expected.

The significant enhancements that are provided when migrating from the MPC500 family to the MPC5500 family are the options for Application Processing Units to enhance specific performance (such as context management or signal processing capability). In addition, there are higher operating speeds and a re-architected CPU to more efficiently feed the CPU. With every generation of new embedded controller there is also better EMC performance and more highly integrated peripherals that can squeeze more and more flash into tighter dimensions. ***